In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A shift overflow detection circuit for a shifter having a data bit length of M and a shift control value bit length of N comprising:

a plurality of circuit elements disposed in M rows and N columns, each circuit element(i,d) of the i-th row and the d-th column having two inputs and an output, a circuit element of a last column generating an output of said shift overflow detection circuit, wherein:

if $d=2^n*2^i$ where n is in the range $1 \leq n \leq ((M/2^{i+1})-1)$, then element(i,d) is an OR gate having a first input connected to said output of element$(i-1,d+2^i)$ and a second input connected to said output of element(i-1,d),

if $d=2^n*2^i+2^j$ where n is in the range $1 \leq n \leq ((M/2^{i+1})-1)$ and j is in the range $0 \leq j \leq i-1$, then element(i,d) is a multiplexer having a first input connected to said output of element(i-1,d), a second input connected to said output of element$(i-1,d+2^i)$ and a control input receiving the i-bit of said shift control value,

if $d=(2^n+1)*2^i$, where n is in the range $1 \leq n \leq ((M/2^{i+1})-1)$ and j is in the range $0 \leq j \leq i-1$, then element(i,d) is a multiplexer having a first input connected to said output of element(i-1,d), a second input receiving 0 and a control input receiving the i-bit of said shift control value, and

for all other combinations of i and d, there is no element(i,d).

2. (Original) The shift overflow detector of claim 1, wherein:

each multiplexer includes

a first pass gate having a input connected to said first input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a first polarity whereby said first pass gate is conducting when said control input is 1, and

a second pass gate having a input connected to said second input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a second polarity opposite to said first polarity whereby said first pass gate is conducting when said control input is 0.

3. (Currently Amended) A shift overflow detection circuit having a 16 bit data length [D15:D0] and a shift control value of 4 bits [S3:S0], comprising:

a first multiplexer having a first input receiving data bit D1, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a first OR gate having a first input receiving data bit D2, a second input receiving data bit D3 and an output;

a second multiplexer having a first input receiving data bit D3, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a second OR gate having a first input receiving data bit D4, a second input receiving data bit D5 and an output;

a third multiplexer having a first input receiving data bit D5, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a third OR gate having a first input receiving data bit D6, a second input receiving data bit D7 and an output;

a fourth multiplexer having a first input receiving data bit D7, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a fourth OR gate having a first input receiving data bit D8, a second input receiving data bit D9 and an output;

a fifth multiplexer having a first input receiving data bit D9, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a fifth OR gate having a first input receiving data bit D10, a second input receiving data bit D11 and an output;

a sixth multiplexer having a first input receiving data bit D11, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a sixth OR gate having a first input receiving data bit D12, a second input receiving data bit D13 and an output;

a seventh multiplexer having a first input receiving data bit D13, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a seventh OR gate having a first input receiving data bit D14, a second input receiving data bit D15 and an output;

an eighth multiplexer having a first input receiving data bit D15, a second input receiving 0, a control input receiving shift value bit S0 and an output;

a ninth multiplexer having a first input connected to said output of said first multiplexer, a second input connected to said output of said second multiplexer, a control input receiving shift control value bit S1 and an output;

a tenth multiplexer having a first input connected to said output of said first OR gate, a second input receiving 0, a control input receiving shift control value bit S1 and an output;

an eighth OR gate having a first input connected to said output of said second OR gate, a second ~~output~~ input connected to said output of said third OR gate and an output;

an eleventh multiplexer having a first input connected to said output of said third multiplexer, a second input connected to said output of said fourth multiplexer, a control input receiving shift control value bit S1 and an output;

a twelfth multiplexer having a first input connected to said output of said third OR gate, a second input receiving 0, a control input receiving shift control value bit S1 and an output;

a ninth OR gate having a first input connected to said output of said fourth OR gate, a second output connected to said output of said fifth OR gate and an output;

a thirteenth multiplexer having a first input connected to said output of said fifth multiplexer, a second input connected to said output of said sixth multiplexer, a control input receiving shift control value bit S1 and an output;

a fourteenth multiplexer having a first input connected to said output of said fifth OR gate, a second input receiving 0, a control input receiving shift control value bit S1 and an output;

a tenth OR gate having a first input connected to said output of said sixth OR gate, a second output connected to said output of said seventh OR gate and an output;

a fifteenth multiplexer having a first input connected to said output of said seventh multiplexer, a second input connected to said output of said eighth multiplexer, a control input receiving shift control value bit S1 and an output;

a sixteenth multiplexer having a first input connected to said output of said seventh OR gate, a second input receiving 0, a control input receiving shift control value bit S1 and an output;

a seventeenth multiplexer having a first input connected to said output of said ninth multiplexer, a second input connected to

said output of said eleventh multiplexer, a control input receiving shift control value bit S2 and an output;

an eighteenth multiplexer having a first input connected to said output of said tenth multiplexer, a second input connected to said output of said twelfth multiplexer, a control input receiving shift control value bit S2 and an output;

a nineteenth multiplexer having a first input connected to said output of said eighth OR gate, a second input receiving 0, a control input receiving shift control value bit S2 and an output;

an eleventh OR gate having a first input connected to said output of said ninth OR gate, a second output connected to said output of said tenth OR gate and an output;

a twentieth multiplexer having a first input connected to said output of said thirteenth multiplexer, a second input connected to said output of said fifteenth multiplexer, a control input receiving shift control value bit S2 and an output;

a twenty first multiplexer having a first input connected to said output of said fourteenth multiplexer, a second input connected to said output of said sixteenth multiplexer, a control input receiving shift control value bit S2 and an output;

a twenty second multiplexer having a first input connected to said output of said tenth OR gate, a second input receiving 0, a control input receiving shift control value bit S2 and an output;

a twenty third multiplexer having a first input connected to said output of said seventeenth multiplexer, a second input connected to said output of said twentieth multiplexer, a control input receiving shift control value bit S3 and an output;

a twenty fourth multiplexer having a first input connected to said output of said eighteenth multiplexer, a second input connected to said output of said twenty first multiplexer, a control input receiving shift control value bit S3 and an output;

a twenty fifth multiplexer having a first input connected to said output of said nineteenth multiplexer, a second input connected to said output of said twenty second multiplexer, a control input receiving shift control value bit S3 and an output;

a twenty sixth multiplexer having a first input connected to said output of said eleventh OR gate, a second input receiving 0, a control input receiving shift control value bit S3 and an output;

a twelfth OR gate having a first input connected to said output of said twenty third multiplexer, a second input connected to said output of said twenty fourth multiplexer and an output;

a thirteenth OR gate having a first input connected to said output of said twenty fifth multiplexer, a second input connected to said output of said twenty sixth multiplexer and an output; and

a fourteenth OR gate having a first input connected to said output of said twelfth OR gate, a second input connected to said output of said thirteenth OR gate and an output forming an output of said shift overflow detection circuit.

4. (Currently Amended) The shift overflow detector of claim 2, wherein:

each of said first ~~to~~ multiplexer, said second multiplexer, said third multiplexer, said fourth multiplexer, said fifth multiplexer, said sixth multiplexer, said seventh multiplexer, said eighth multiplexer, said ninth multiplexer, said tenth multiplexer, said eleventh multiplexer, said twelfth multiplexer, said thirteenth multiplexer, said fourteenth multiplexer, said fifteenth multiplexer, said sixteenth multiplexer, said seventh multiplexer, said eighteenth multiplexer, said nineteenth multiplexer, said twentieth multiplexer, said twenty first multiplexer, said twenty second multiplexer, said twenty third multiplexer, said twenty fourth multiplexer, said twenty fifth multiplexer and said twenty sixth multiplexer includes

a first pass gate having a input connected to said first input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a first polarity whereby said first pass gate is conducting when said control input is 1, and

a second pass gate having a input connected to said second input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a second polarity opposite to said first polarity whereby said first pass gate is conducting when said control input is 0.

5. (Currently Amended) A shift overflow detection circuit having a 32 bit data length [D31:D0] and a shift control value of 5 bits [S4:S0], comprising:

a first multiplexer having a first input receiving data bit D1, a second input receiving data bit D3, a control input receiving shift control value bit S1 and an output;

a first NAND gate having a first input connected to said output of said first multiplexer, a second input receiving shift control value bit S0 and an output;

a first OR gate having a first input receiving data bit D2, a second input receiving data bit D3 and an output;

a second NAND gate having a first input connected to said output of said first OR gate, a second input receiving shift control value bit S0 and an output;

a first NOR gate having a first input receiving data bit D4, a second input receiving data bit D5 and an output;

a second multiplexer having a first input receiving data bit D5, a second input receiving data bit D7, a control input receiving shift control value bit S1 and an output;

a third NAND gate having a first input connected to said output of said second multiplexer, a second input receiving shift control value bit S0 and an output;

a second NOR gate having a first input receiving data bit D6, a second input receiving data bit D7 and an output;

a second OR gate having a first input receiving data bit D6, a second input receiving data bit D7 and an output;

a fourth NAND gate having a first input connected to said output of said second OR gate, a second input receiving shift control value bit S0 and an output;

a third NOR gate having a first input receiving data bit D8, a second input receiving data bit D9 and an output;

a third multiplexer having a first input receiving data bit D9, a second input receiving data bit D11, a control input receiving shift control value bit S1 and an output;

a fifth NAND gate having a first input connected to said output of said third multiplexer, a second input receiving shift control value bit S0 and an output;

a fourth NOR gate having a first input receiving data bit D10, a second input receiving data bit D11 and an output;

a third OR gate having a first input receiving data bit D10, a second input receiving data bit D11 and an output;

a sixth NAND gate having a first input connected to said output of said third OR gate, a second input receiving shift control value bit S0 and an output;

a fifth NOR gate having a first input receiving data bit D12, a second input receiving data bit D13 and an output;

a fourth multiplexer having a first input receiving data bit D13, a second input receiving data bit D15, a control input receiving shift control value bit S1 and an output;

a seventh NAND gate having a first input connected to said output of said fourth multiplexer, a second input receiving shift control value bit S0 and an output;

a sixth NOR gate having a first input receiving data bit D14, a second input receiving data bit D15 and an output;

a fourth OR gate having a first input receiving data bit D14, a second input receiving data bit D15 and an output;

an eighth NAND gate having a first input connected to said output of said fourth OR gate, a second input receiving shift control value bit S0 and an output;

a seventh NOR gate having a first input receiving data bit D16, a second input receiving data bit D17 and an output;

a fifth multiplexer having a first input receiving data bit D17, a second input receiving data bit D19, a control input receiving shift control value bit S1 and an output;

a ninth NAND gate having a first input connected to said output of said fifth multiplexer, a second input receiving shift control value bit S0 and an output;

an eighth NOR gate having a first input receiving data bit D18, a second input receiving data bit D19 and an output;

a fifth OR gate having a first input receiving data bit D18, a second input receiving data bit D19 and an output;

a tenth NAND gate having a first input connected to said output of said fifth OR gate, a second input receiving shift control value bit S0 and an output;

a ninth NOR gate having a first input receiving data bit D20, a second input receiving data bit D21 and an output;

a sixth multiplexer having a first input receiving data bit D21, a second input receiving data bit D23, a control input receiving shift control value bit S1 and an output;

an eleventh NAND gate having a first input connected to said output of said sixth multiplexer, a second input receiving shift control value bit S0 and an output;

a tenth NOR gate having a first input receiving data bit D22, a second input receiving data bit D23 and an output;

a sixth OR gate having a first input receiving data bit D22, a second input receiving data bit D23 and an output;

a twelfth NAND gate having a first input connected to said output of said sixth OR gate, a second input receiving shift control value bit S0 and an output;

an eleventh NOR gate having a first input receiving data bit D24, a second input receiving data bit D25 and an output;

a seventh multiplexer having a first input receiving data bit D25, a second input receiving data bit D27, a control input receiving shift control value bit S1 and an output;

a thirteenth NAND gate having a first input connected to said output of said seventh multiplexer, a second input receiving shift control value bit S0 and an output;

a twelfth NOR gate having a first input receiving data bit D26, a second input receiving data bit D27 and an output;

a seventh OR gate having a first input receiving data bit D26, a second input receiving data bit D27 and an output;

a fourteenth NAND gate having a first input connected to said output of said seventh OR gate, a second input receiving shift control value bit S0 and an output;

a thirteenth NOR gate having a first input receiving data bit D28, a second input receiving data bit D29 and an output;

an eighth multiplexer having a first input receiving data bit D29, a second input receiving data bit D31, a control input receiving shift control value bit S1 and an output;

a fifteenth NAND gate having a first input connected to said output of said eighth multiplexer, a second input receiving shift control value bit S0 and an output;

a fourteenth NOR gate having a first input receiving data bit D30, a second input receiving data bit D31 and an output;

an eighth OR gate having a first input receiving data bit D30, a second input receiving data bit D31 and an output;

a sixteenth NAND gate having a first input connected to said output of said eighth OR gate, a second input receiving shift control value bit S0 and an output;

a seventeenth NAND gate having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate, a third input connected to said output of said first NOR gate, a fourth input connected to said output of said second NOR gate and an output;

an eighteenth NAND gate having a first input connected to said output of said third NAND gate, a second input connected to said output of said fourth NAND gate and an output;

a nineteenth NAND gate having a first input connected to said output of said third NOR gate, a second input connected to said output of said fourth NOR gate, a third input connected to said output of said fifth NOR gate, a fourth input connected to said output of said sixth NOR gate and an output;

a twentieth NAND gate having a first input connected to said output of said fifth NAND gate, a second input connected to said output of said sixth NAND gate, a third input connected to said output of said fifth NOR gate, a fourth input connected to said output of said sixth NOR gate and an output;

a twenty first NAND gate having a first input connected to said output of said seventh NAND gate, a second input connected to said output of said eighth NAND gate and an output;

a twenty second NAND gate having a first input connected to said output of said seventh NOR gate, a second input connected to said output of said eighth NOR gate, a third input connected to said output of said ninth NOR gate, a fourth input connected to said output of said tenth NOR gate and an output;

a twenty third NAND gate having a first input connected to said output of said ninth NAND gate, a second input connected to said output of said tenth NAND gate, a third input connected to said output of said ninth NOR gate, a fourth input connected to said output of said tenth NOR gate and an output;

a twenty fourth NAND gate having a first input connected to said output of said eleventh NAND gate, a second input connected to said output of said twelfth NAND gate and an output;

a twenty fifth NAND gate having a first input connected to said output of said eleventh NOR gate, a second input connected to said output of said twelfth NOR gate, a third input connected to said output of said thirteenth NOR gate, a fourth input connected to said output of said fourteenth NOR gate and an output;

a twenty sixth NAND gate having a first input connected to said output of said thirteenth NAND gate, a second input connected to said output of said fourteenth NAND gate, a third input connected to said output of said thirteenth NOR gate, a fourth input connected to said output of said fourteenth NOR gate and an output;

a twenty seventh NAND gate having a first input connected to said output of said fifteenth NAND gate, a second input connected to said output of said sixteenth NAND gate and an output;

a seventeenth multiplexer having a first input connected to said output of said nineteenth NAND gate, a second input connected to said twenty fifth NAND gate, a control input receiving shift control value bit S4 and an output;

a twenty eighth NAND gate having a first input connected to said output of said seventeenth multiplexer, a second input receiving shift control value bit S3 and an output;

a ninth OR gate having a first input connected to said output of said twenty second NAND gate, a second input connected to said output of said twenty fifth NAND gate and an output;

a twenty ninth NAND gate having a first input connected to said output of said ninth OR gate, a second input receiving shift control value bit S4 and an output;

an inverting multiplexer having a first input connected to said output of said seventeenth NAND gate, a second input connected to said output of said eighteenth NAND gate, a third input connected to said output of said twentieth NAND gate, a fourth input connected to said output of said twenty first NAND gate, a fifth input connected to said output of said twenty third NAND gate, a sixth input connected to said output of said twenty fourth NAND gate, a seventh input connected to said output of said twenty sixth NAND gate, an eighth input connected to said output of said twenty seventh NAND gate, three control ~~input~~ inputs receiving respective shift control value bits S4, S3 and S2 and an output, whereby said inverting multiplexer outputs a inverted first input if said shift control bits S4, S3 and S2 are "111", a inverted second input if said shift control bits S4, S3 and S2 are "110", a inverted third input if said shift control bits S4, S3 and S2 are "101", a inverted fourth input if said shift control bits S4, S3 and S2 are "100", a inverted fifth input if said shift control bits S4, S3 and S2 are "011", a inverted sixth input if said shift control bits S4, S3 and S2 are "010", a inverted seventh input if said shift control bits S4, S3 and S2 are "001" and a inverted eighth input if said shift control bits S4, S3 and S2 are "000"; and

a thirtieth NAND gate having a first input connected to said output of said inverting multiplexer, a second input connected to said output of said twenty eighth NAND gate, a third input connected to said output of said twenty ninth NAND gate and an output forming an output of said shift overflow detection circuit.

6. (Original) The shift overflow detector of claim 5, wherein: each of said first to seventeenth multiplexer includes

a first pass gate having a input connected to said first input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a first polarity whereby said first pass gate is conducting when said control input is 1, and

a second pass gate having a input connected to said second input of said multiplexer, an output connected to said output of said multiplexer and receiving said control input in a second polarity opposite to said first polarity whereby said first pass gate is conducting when said control input is 0.

7. (Original) The shift overflow detector of claim 5, wherein: said inverting multiplexer includes

a first inverter having a input receiving shift control value bit S2 and an output,

a second inverter having a input receiving shift control value bit S3 and an output,

a third inverter having a input receiving shift control value bit S4 and an output,

a first NAND gate having a first input receiving shift control value S2, a second input receiving shift control value S3, a third input receiving shift control value S4 and an output,

a second NAND gate having a first input connected to said output of said first inverter, a second input receiving shift control value S3, a third input receiving shift control value S4 and an output,

a third NAND gate having a first input receiving shift control value S2, a second input connected to said output of said second inverter, a third input receiving shift control value S4 and an output,

a fourth NAND gate having a first input connected to said output of said first inverter, a second input connected to said output of said second inverter, a third input receiving shift control value S4 and an output,

a fifth NAND gate having a first input receiving shift control value S2, a second input receiving shift control value S3, a third input connected to said output of said third inverter and an output,

a sixth NAND gate having a first input connected to said output of said first inverter, a second input receiving shift control value S3, a third input connected to said output of said third inverter and an output,

a seventh NAND gate having a first input receiving shift control value S2, a second input connected to said output of said second inverter, a third input connected to said output of said third inverter and an output,

a eighth NAND gate having a first input connected to said output of said first inverter, a second input connected to said output of said second inverter, a third input connected to said output of said third inverter and an output,

a fourth inverter having an input connected to said output of said first NAND gate and an output,

a fifth inverter having an input connected to said output of said second NAND gate and an output,

a sixth inverter having an input connected to said output of said third NAND gate and an output,

a seventh inverter having an input connected to said output of said fourth NAND gate and an output,

a eighth inverter having an input connected to said output of said fifth NAND gate and an output,

a ninth inverter having an input connected to said output of said sixth NAND gate and an output,

a tenth inverter having an input connected to said output of said seventh NAND gate and an output,

a eleventh inverter having an input connected to said output of said eighth NAND gate and an output,

a first pass gate having an input connected to said first input of said inverting multiplexer, a first control input connected to said output of said first NAND gate, a second control input connected to said output of said fourth inverter and an output,

a second pass gate having an input connected to said second input of said inverting multiplexer, a first control input connected to said output of said second NAND gate, a second control input connected to said output of said fifth inverter and an output,

a third pass gate having an input connected to said third input of said inverting multiplexer, a first control input connected to said output of said third NAND gate, a second control input connected to said output of said sixth inverter and an output,

a fourth pass gate having an input connected to said fourth input of said inverting multiplexer, a first control input connected to said output of said fourth NAND gate, a second control input connected to said output of said seventh inverter and an output,

a fifth pass gate having an input connected to said fifth input of said inverting multiplexer, a first control input connected to said output of said fifth NAND gate, a second control input connected to said output of said eighth inverter and an output,

a sixth pass gate having an input connected to said sixth input of said inverting multiplexer, a first control input connected to said output of said sixth NAND gate, a second control input connected to said output of said ninth inverter and an output,

a seventh pass gate having an input connected to said seventh input of said inverting multiplexer, a first control input connected to said output of said seventh NAND gate, a second control input connected to said output of said tenth inverter and an output,

an eighth pass gate having an input connected to said eighth input of said inverting multiplexer, a first control input connected to said output of said eighth NAND gate, a second control input connected to said output of said eleventh inverter and an output, and

a twelfth inverter having an input connected to said output of said first, second, third, fourth, fifth, sixth, seventh and eighth pass gates and an output forming said output of said inverting multiplexer.